Monolayer doping and other strategies in high surface-to-volume ratio silicon devices

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Abstract

To maintain electron device scaling, in recent years the semiconductor industry has been forced to move from planar to non-planar thin-body electron device architectures. This alone has created the need to develop a radically new, non-destructive, conformal method for doping. Doping alters the electrical properties of a semiconductor, related to the access resistance. Monolayer doping (MLD) is a promising surface-based technique, whereby organic molecules are covalently bound to the semiconductor surface at relatively low processing temperatures (room temperature – 160 °C). A thermal treatment is then applied which both frees the dopant atoms from the organic molecules, and provides the energy for diffusion into the semiconductor substrate and subsequent activation. Very promising results have been achieved, but mostly on planar unpatterned substrates. There is now a need to assess the suitability of MLD for thin-body semiconductor features with high surface-to-volume ratios and densely packed structures. It is the aim of this review paper to consider MLD from this perspective.

I. Introduction

The semiconductor industry has been based, for the last 40 years, on incremental scaling of device dimensions to achieve performance gains [1]. The principal economic benefit of such an approach is that it allows the industry to fully apply previous technology investments to future products. However, developmentally, scaling is not a linear process. It has been required at certain points to make dramatic adjustments to the technology design or process steps to maintain Moore's Law [2]. For example, the transition from planar to three dimensional device geometries [3] extended the lifetime of Moore's Law by several device generations.

Figure 1 shows the ITRS predictions for five generations of technology node [4]. The channel length and fin diameter will continue to scale but the most dramatic scaling is associated with fin pitch. This level of scaling combined with non-planar geometry present problems for ion implantation, the state-of-the-art in semiconductor doping. Ion implantation is the industry standard because it can generate a single ion species with a single energy in an industrially friendly, highly controlled fashion [5], The problems associated with it are crystal damage of the semiconductor as the energetic atoms strike the target, and the extremely directional nature of the process, leading to a lack of conformality in non-planar structures. For fin devices with sub-10 nm diameters, crystal damage will be difficult to anneal out and for smaller fin pitches the shadowing effect of ion implantation will lead to highly non-conformal doping profiles.

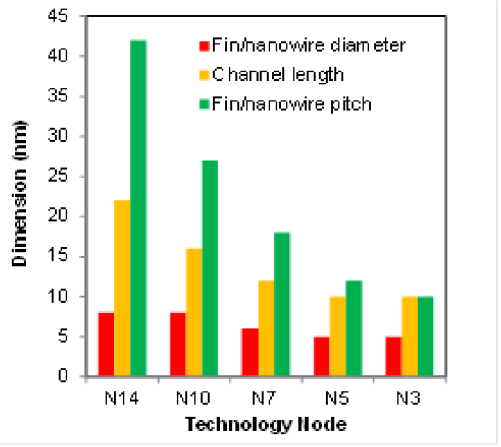

Figure 1: ITRS predictions enabling More Moore. Very small changes in fin/nanowire diameters are predicted with much larger concurrent changes in pitch scaling.

In our group we have expertise in a non-destructive and conformal diffusion-doping process known as monolayer doping (MLD) [6-9], but most of that work has been done on planar substrates, the next step is to benchmark ion implantation against MLD to test its viability as an alternative for tightly pitched fins with sub-10 nm diameters.

Interestingly, for devices down to 10 nm ion implantation has shown superior performance to MLD, even though cross-section TEM characterisation showed the ion implanted fins were highly defective. This can be explained by a key MLD limitation. Figure 2 shows the maximum active carrier concentration is currently limited to 2×10^{19} atoms/cm^3 for standard MLD doping using P as the dopant source. Note, P is the most commonly studied n-type dopant

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for MLD to date. This result has been replicated by other research groups. Extensive examination of the literature also reveals that active carrier concentrations of $>2\times10^{19}$ atoms/cm^3 have not been achieved [10, 11]. This result is rather surprising as this concentration is well below the solid solubility of P in silicon. It is postulated that interfacial trapping in an oxide is part of the problem [12, 13].

Though this limitation has been identified (threshold doping carrier concentration needs to be $>1\times10^{20}$ atoms/cm^3) it is not believed to be insurmountable, and steps are currently being taken to improve the situation. The non-destructive, controlled and conformal benefits of the process make developing methods to overcome this roadblock a worthwhile investment of time and expertise.

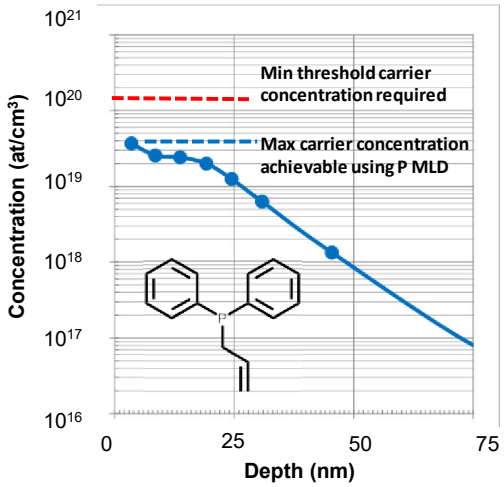

Figure 2: Carrier concentration profile vs depth using P MLD (blue line) & min threshold carrier concentration required (red line). Inset shows the molecule used for MLD.

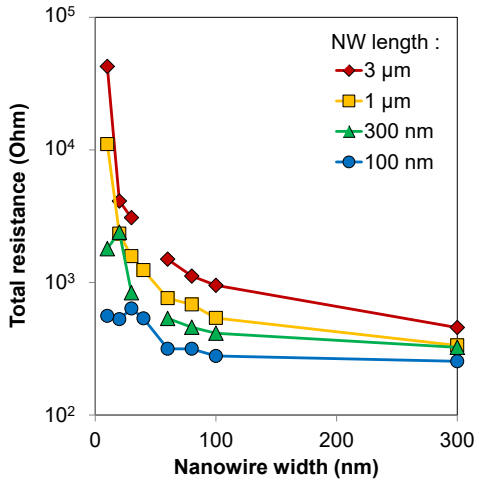

Figure 3: Total resistance of nanowires versus width for ion implantation of P for nanowires of varied lengths.

Ion implantation will become obsolete. There is a diminished electrical performance of smaller nanowires doped in this way (Figure 3). Therefore, an alternative method for doping that is conformal and non-destructive will be required. MLD has been successfully used to dope semiconductor nanowires with sub-10 nm diameters and is non-destructive.

Finally, dopant incorporation in silicon can be done in-situ during epitaxial growth, or ex-situ for localized material modification using a variety of sources including ion, solid, liquid, or gas. The advantages and disadvantages of the state-of-the-art doping is summarized below in Figure 4. In the next section we will discuss the opportunities and limitations of MLD in more detail.

	Beamline Ion Implant	Plasma Doping	MLD
PRO	Industry standard Single ion energy Single species	Less damage than beamline Better conformality than beamline	No damage Conformal
CON	Crystal damage Too directional for conformal doping	Under development Multiple ion energies and species Surface quality	Least mature Needs boost in dopant activation levels

Figure 4: A brief comparison of different doping strategies.

II Monolayer doping capability for future silicon devices

MLD can be compared to the alternative doping techniques under a number of categories. In this section we will focus on issues mainly directed at dense-pitch nanowire devices. Specifically, we consider MLD under the following headings; processing temperature, dopant conformality, carbon contamination, surface integrity and smoothness, wetting, dose control, dopant diffusion control, thermal stability, and oxidation prevention.

A. Processing temperature

One of the main advantages of MLD is that it is a low-temperature process, typically processing is done at room temperature or at elevated temperatures in the order of 160 °C. In comparison, in-situ doped epitaxial growth has a significant thermal budget, while the temperature required to prevent damage accumulation during ion implantation is in the range of 400 °C [14,15]. This could be considered the technology norm for modern FinFET and MugFET device processing, but this high temperature adds process complexity, and thus adds cost. For example standard photoresists cannot tolerate 400 °C so a hard-mask process must be developed and used. Furthermore where co-integration or 3D stacking of different materials is being considered, the overall thermal budget must be tightly controlled and minimized.

B. Dopant conformality

This problem can be simplified as "getting dopants in the sidewalls" [16], because getting the dopant in the top surface is relatively easy using conventional methods. It is well known at this stage that ion implantation, and plasma doping to a lesser degree, are highly directional. Firing bullets at a target is the usual analogy. This directionality is a killer for conformal doping of high aspect ratio tall fins in FinFETs and MugFETs. Shadowing by neighboring fins can cause poor sidewall coverage and dopant incorporation, and hence leads to local variations in dopant activation and resistance, which is undesirable for device behavior for a number of reasons including device variability and drive current performance. Some straightforward simulations of ion implantation into densely packed tall features can highlight the problem.

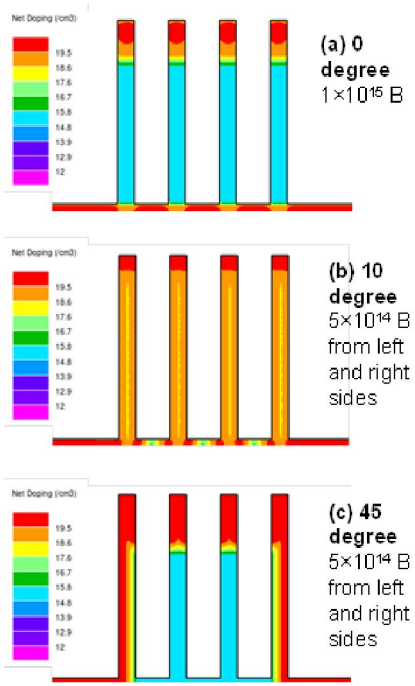

Figure 5: The problem of choosing the right implant angle when implanting into dense tall structures. (a) a 0 degree implant only dopes from the top and the sidewalls do not incorporate dopants, (b) a 10 degree implant produces some sidewall incorporation but it is not ideal, (c) a 45 degree implant can produce high sidewall incorporation, but shadowing is severe and there is a high degree of asymmetry in the doping distributions.

Shown in Fig. 5 is a comparison of three different implant angles. The angle is relative to the top surface. A 0 degree implant only dopes from the top surface and the sidewalls do not incorporate dopants, a 10 degree implant produces some sidewall incorporation but it is not ideal, while a 45 degree implant can produce high sidewall incorporation, but shadowing is severe and there is a high degree of asymmetry in the doping distributions.

MLD, on the other hand, is a surface-based technique, whereby molecules with molecular footprint on the order of 1 nm are brought into contact with a substrate. In principle, these molecules should be able intercalate into densely pitched structures and under the right conditions react with and form a covalent bond with the surface atoms. So, being a surface reaction-based technique line-of-sight issues that other doping approaches struggle with, should be resolved. Irrespective of the nanowire or fin shape and dimension, the molecules should bind to each surface.

C. Carbon contamination

One of the unresolved issues for MLD is what happens to the C during the drive-in anneal. This question is essentially untouched in the literature. The dopant atoms may be freed by the organic molecules and diffuse into the substrate, but does the C stay on the surface? Does it get incorporated in the capping layer? Does it in-diffuse to the substrate along with the dopant atoms? If so, does it diffuse faster or slower than the diffusing dopant atoms?

For electron devices there are two major concerns with the C from MLD. Firstly, if the C stays at the surface this will make any subsequent source/drain epi growth difficult, as usually this growth requires a highly cleaned surface to begin with. Clearly, large amounts of surface C will be problematic. In modem MOSFETs the source/drain epi is important prior to contact formation in order to reduce contact resistance, which is becoming the largest parasitic resistance and subsequently the current-limiting factor in MOSFET devices.

Secondly, C could be a problem if it in-diffuses very quickly in large quantities. This will depend on the C diffusivity and solid solubility in the host substrate. From a MOSFET device perspective, if large amounts of C diffuse faster than the dopants, and hence reside in a reverse biased depletion region of a p-n junction, significant reverse-bias leakage current could arise [17]. This leakage current is undesirable, as it hinders low-power operation for MOS devices, as well as increasing stand-by leakage current and poor battery lifetimes in hand-held portable electronic products. It is well known that impurities and crystal defects can induce leakage currents in MOS devices [18-20]. Furthermore carrier lifetimes and non-ideal leakage currents can be considered as an effective monitor for process induced defects and for the processing history of the junction [21].

D. Surface integrity and smoothness

Perhaps one of the most important aspects missing from the MLD discussion in the literature is the quality of the surface post-processing. Surface smoothness and integrity is a key factor for proper control of MLD in terms of it being a reproducible and viable process. This process is being developed for

technology that is 10 nm and below. To put this in perspective, a 10 nm width is only approximately 40 Si atoms wide. In order to maintain the device integrity, atomic smoothness, or close to, is required. Consider, even, that a native oxide is ~1 nm thick, its removal (1 nm from either side of a 10 nm device) results in a 20 % variation on device width. Chemistry-based processes have the potential to allow precise control over the surface composition and smoothness. However, even small variations in time and reaction parameters, such as temperature and concentration, can cause integrity issues which will have a dramatic effect on device reliability.

Most MLD studies in the public domain have been on unpatterned blanket substrates, which makes sense, in order to build up understanding of the chemistry and physics involved. Blanket substrates are needed to extract chemical and active doping profiles, by Secondary Ion Mass Spectrometry, Spreading Resistance Profiling, or Electrochemical Capacitance-Voltage profiling which either sputter or etch a crater into a planar surface. However, very few reports of surface roughness analysis have been presented. If chemical processing introduces significant surface roughness (>1nm) then it is not suitable for transfer to nanowire devices. MLD has matured to a point where it needs to be studied on scaled, thin-body semiconductor structures and devices.

There are a number of practical consequences for a roughened surface during or post-MLD processing. A rough surface has a greater surface area than a smooth planar surface and thus potentially more sites for covalent bonding of organic molecules. This may have an apparent benefit, as more bound molecules should give a greater supply of dopant atoms, and thus higher dopant concentrations post drive-in anneal. This may not be an issue for planar devices where there is a low surface-to-volume ratio or even in the raised source and drain regions of FinFET and MugFET devices. However, if there is surface attack and roughening while applying the process to scaled features, such as sub-10 nm diameter nanowires, this has major consequences for the device, as shown in Figure 6(b). As well as introducing an element of randomness, which leads to poor reproducibility, this will lead to device-to-device variability, and across wafer variability possibly. In extreme cases this effect could lead to total disintegration of nanowires where there is a high surface-to-volume ratio. This is a major issue for MLD and must be addressed in future MLD studies.

Finally as the technology heads towards gate-all-around devices, Si features will be free-floating and released from the underlying substrate. This alone throws up a new set of challenges for any process, including doping, as these sub-10 nm features will be susceptible to structural deformation, like that in Figure 6(c), which if uncontrolled will lead to problems of poor variability and yield.

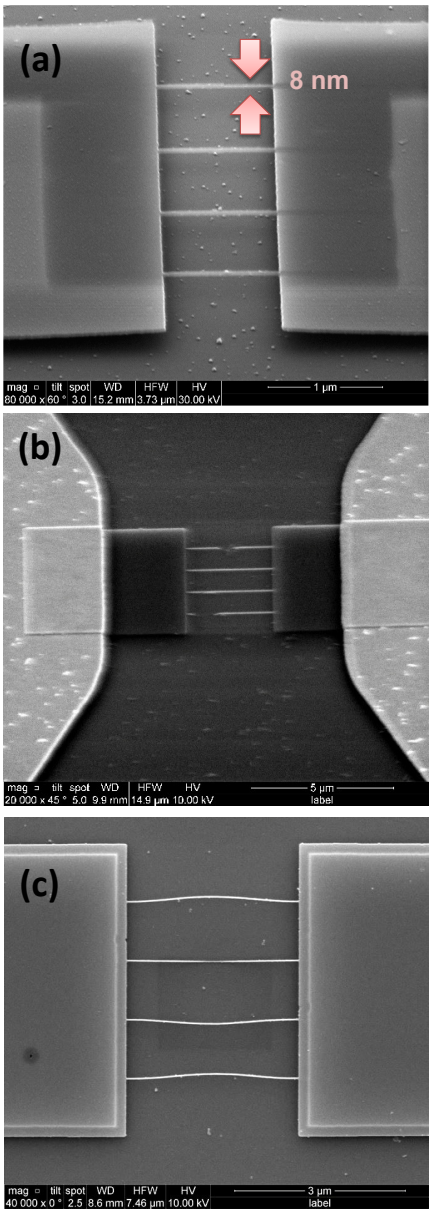

Figure 6: Challenges working with sub-10nm Si structures, (a) shows a representative SEM image of well-behaved Si nanowires released from the substrate, (b) shows nanowires attacked by the doping process, as these structures have such a high surface-to-volume ratio any surface attack will be extreme, (c) for gate-all-around nanowires released from a substrate the processing should not induce any stress, as these features will buckle and bend in an uncontrolled way.

E. Wetting

For the most part to date MLD is a liquid-based chemistry process. The benefit of liquid-based chemistry is that there are far more potential viable precursors. In liquid-based chemistry a solution of the target molecule (containing the dopant atom) and a solvent is prepared. In order for the reaction to take place this solution must be able wet the target substrate. By supplying energy, (e.g. in the form of heat or UV light) when the dissolved molecules come

into contact with the substrate they will react and form a covalent bond. In a predetermined amount of time, dependent on the rate of reaction, all available reaction sites will have a molecule containing the dopant atom attached. On planar substrates, single-fin structures, or arrays with relaxed pitches, this is a relatively straightforward process as the solution containing the molecule should be able come into contact with all the surfaces.

A more challenging concern however will be as MugFET fins are patterned closer together and nanowire device pitches are scaled, whether the solution will be able intercalate and wet between the fin structures (Figure 7). Issues such as surface tension start to come into play. There will come a point where pitches and spaces are just too small for liquid-based chemistry. This must be addressed because, from a device point of view, nanowires and fins are going to continue to become more and more densely packed in order to facilitate future electron device scaling.

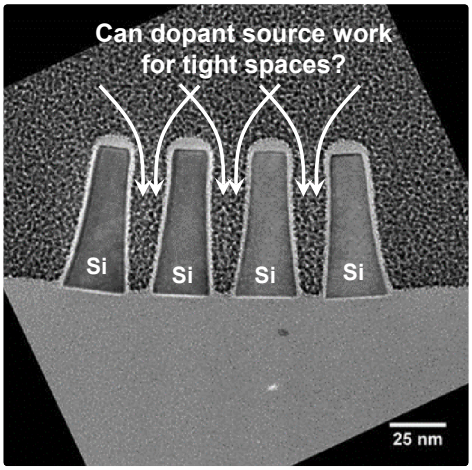

Figure 7: A representative TEM image of a tight pitch four Si nanowire device, where the spacing between the nanowires is 12 nm at the base of the structures. Such tight spaces with high aspect ratios present a whole new set of challenges for process technologies.

F. Dose control

One of the strengths of ion implantation is that it can control dose to a very high degree. There are decades of engineering skill and effort behind this, but nevertheless it is a key aspect when doping semiconductors. There have been a number of reported methods for controlling MLD dosages, that have been experimentally demonstrated, including molecule design, and surface oxide thickness variations. Monolayer doping offers a unique method for controlling the dose and potentially with great accuracy. The molecule of choice can be designed to form a self-limiting monolayer on the chosen substrate. Below in Figure 8 is a schematic representation of an ideally ordered monolayer. To a good approximation the footprint of the target molecule can be calculated and the potential dose extrapolated. You can back-calculate the required dose and design a molecule with a footprint that can deliver that dose. The footprint of the molecule will have a dramatic effect of the dose delivered.

Other methods of controlling the dose are by doing repeated cycles of MLD on the device. Or by incorporation of non-dopant containing molecules, or multiple dopant containing molecules. They are ultimately methods by which the dose can be controlled using MLD.

G. Dopant diffusion control

Stated at the outset, one of the challenges around doping semiconductors is the dopant diffusion control. MLD is an in-diffusion based process which relies on the thermal budget of the anneal to drive the dopant atoms from the surface into the substrate. At present most MLD studies have been done in conjunction with furnace or rapid-thermal-anneal (RTA) type thermal treatments, which produce relatively deep (>50 nm) doping profiles. By combining MLD with lower thermal budget anneals or with point defect engineering strategies, known in Si and Ge [22-24], shallow doping profiles (<50 nm) should be achievable.

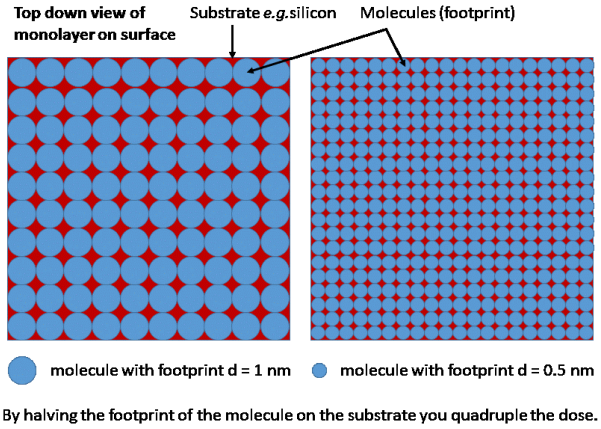

Figure. 8: A schematic representation of an ideally ordered monolayer. To a good approximation the footprint of the target molecule can be calculated and the potential dose extrapolated

H. Thermal stability and oxidation prevention

While the provision of dopant atoms appears to be the primary application of MLD, it should be noted that MLD can serve a surface passivation function at the same time. Surface terminations will affect its reactivity with the ambient. MLD-prepared surfaces have been shown experimentally to prevent oxidation in Si for example. In theory MLD-like techniques could be used to passivate nanowire surfaces in a variety of ways that have not yet been extensively explored.

III. Conclusions

Much innovative work has been performed to date exploring MLD as an alternative doping technique. However most of the work in the literature is based on planar Si substrates, and the work now needs to switch focus on issues mainly directed at dense-pitch nanowire devices. Moreover MLD ought to be evaluated in the future in terms of processing temperature, dopant conformality, carbon contamination, surface integrity and smoothness, wetting, dose control, dopant diffusion control, thermal stability, and oxidation prevention. The gentleness and conformality aspects of MLD are potential advantages over ion implantation, plasma assisted doping and other solid-source doping processes.

Acknowledgements

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